3. (Amended) Ground plane according to claim 1 [or 2], wherein the dielectric layer is an integral part of said chip.

5. (Amended) Ground plane according to claim 3 [or 4], wherein said dielectric layer comprises silicon oxide.

6. (Amended) Ground plane according to [one of the proceeding claims] claim 1, wherein said second capacitor plate comprises a layer of conductive glue.

7. (Amended) Ground plane according to [any of the preceding claims] claim 1, wherein said capacitor plate is a metallic layer on said supporting member.

8. (Amended) Ground plane according to claim [claims] 6 [and 7], wherein said layer of conductive glue is provided between said metallic layer and said dielectric layer.

9. (Amended) Ground plane according to [one of the proceeding claims] claim 1, wherein said at least one electrically conducting via extending through said supporting member is directly connected to the second capacitor plate.

10. (Amended) Ground plane according to claim 7[,8 or 9], wherein said vias and said metallic layer are integrally formed from the same metal.

Please add new claims 17-21 as follows:

-- 17. Ground plane according to claim 2, wherein the dielectric layer is an integral part of said chip.

18. Ground plane according to claim 4, wherein said dielectric layer comprises silicon oxide.

19. Ground plane according to claim 7, wherein said layer of conductive glue is provided between said metallic layer and said dielectric layer.

20. Ground plane according to claim 8, wherein said vias and said metallic layer are integrally formed from the same metal.

21. Ground plane according to claim 9, wherein said vias and said metallic layer are integrally formed from the same metal.--

IN THE ABSTRACT

Line 12, delete "Fig. 1".